Patent claims

1. An electronic phase-locked loop (PLL) for jitter-attenuated clock multiplication, in particular as part of an integrated circuit (IC) for integrated services communications networks (ISDN), data communication or networks in which the frequency of a controllable oscillator (9, DCXO) is set in such a way that it corresponds to a reference frequency (REF CLK), the output signal of the oscillator (DCXO CLK) being compared with the reference frequency in a digital phase detector (1), and the output signal of the digital phase detector (1) setting the frequency of the oscillator (9) via a digital regulated system, characterized in that
the digital phase-locked loop is connected up to an additional analog phase detector (2, APD) and a lock detection (4) for activation.

2. The electronic phase-locked loop (PLL) as claimed in claim 1, characterized in that the digital phase-locked loop comprises a digital phase detector (1), a code converter (4), a PI filter (10), a drive circuit (8, DCXO-control) for the oscillator (9), the oscillator (9, DCXO), which is designed as a digitally controllable crystal oscillator, and a counter (3), the lock detection being undertaken by the code converter (4).

3. The electronic phase-locked loop (PLL) as claimed in claims 1 or 2, characterized by a configuration such that, in the event of transition of the digital phase-locked loop into a limit cycle with a phase error, called jitter, alternating between the values +1, 0 and -1, the limitation of the accuracy is cancelled by the additional analog phase detector (2), the lock detection activating

the analog phase detector (2) via a line (10, "ana_mode"), said analog phase detector thereupon regulating both clock edges of the jitter in a continuously variable manner until said clock edges are synchronous with one another.

4. An integrated circuit (IC) having an electronic phase-locked loop (PLL) of claims 1, 2 or 3.